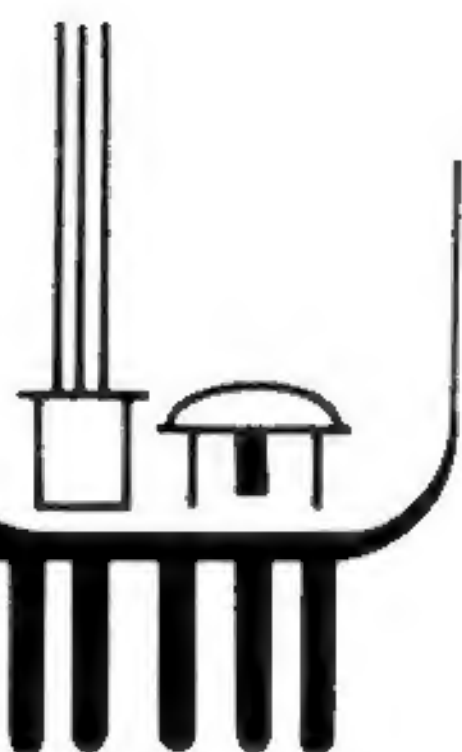


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# experiments with WWVB

Concluding details on receiving methods and syncing Superclock and WWVB

by DON LANCASTER

**TECHNIQUE No. 4—Add a "Flywheel."** This is a sledge hammer trick and adds all sorts of parts and complexity, but it really works well and doesn't cost too much. Essentially, we build a phase-lock loop on the output whose frequency is 1 hertz and whose loop bandwidth is half a minute and is critically damped. The output of the flywheel now drives the decoder.

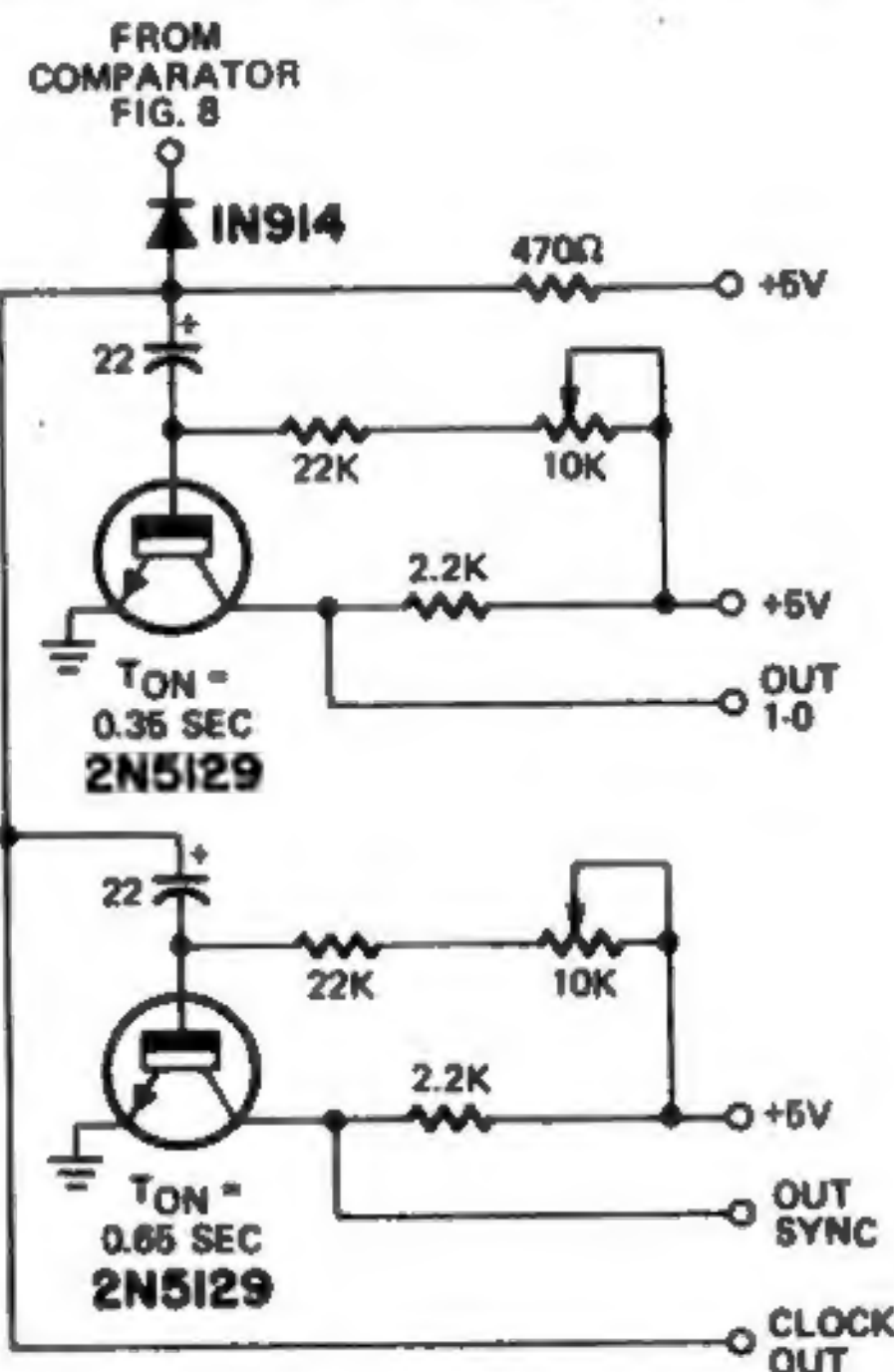
We can go to a 4-Hz VCO and a divide-by-four to get the one second output frequency, and gain a bunch in the "1"-0" identification process. To do this, we decode the first three of the four states. The circuit is shown in Fig. 9.

The first state does the gated phase detection and lasts for a quarter-second time interval between 0.875 seconds on the previous second to 0.125 seconds on the next second. Normally, a sudden drop will occur precisely at 1 second. An early-late error can then be fed to the integrator which averages out a series of early-late commands to get an average error signal which the loop continuously drives to zero.

We then use a second "noise gate" to look for a low state between 0.625 and 0.875 seconds and a final noise gate to look for a low state between 0.375 and 0.625 seconds. The first noise gate tells us if a

pulse is present, while the second noise gate tells us if a "0" is *not* present. Together, we get the detected "1"s and "0"s.

Once we have a reliable signal, we have to decode it and send it to the clock. First, we have to detect 1's, 0's, and pulses. We get these ready to go from the flywheel, or we can add the 1-0 sync detectors shown in Fig. 10 instead. The "1"s and "0"s are marched through the shift register. The sync or detected P pulses detects the double pulse occurring at the beginning of each minute and sets up a two-stage shift register consisting of the third and fourth D-flops in the string. The third register goes high on second No. 2 and drops on second No. 10, with an update for the minutes and seconds being derived on the falling edge. The fourth register goes high on second No. 10 and drops on second No. 20, providing the hours update. The update process will be within a fraction of a second of true WWVB time. For more precision, the input signal can be de-



1-0 & SYNC DETECTORS  
USED IN ABSENCE OF PLL FLYWHEEL

**FIG. 10—SYNC DETECTOR** extracts the 1's and 0's from the WWVB incoming signal.

layed slightly more and eleven seconds can be parallel loaded into the seconds counters at the precise update time. Fig. 11 is the required interface for use between the circuit in Fig. 9 and 10 and Superclock.

### Local conditions

A final note on using the receivers. Some local interference can really wipe the receiver out, so be careful where you put it and how you use it. For instance, if you are within 8 feet of a television set, the horizontal oscillator can cause problems. So

(continued on page 101)

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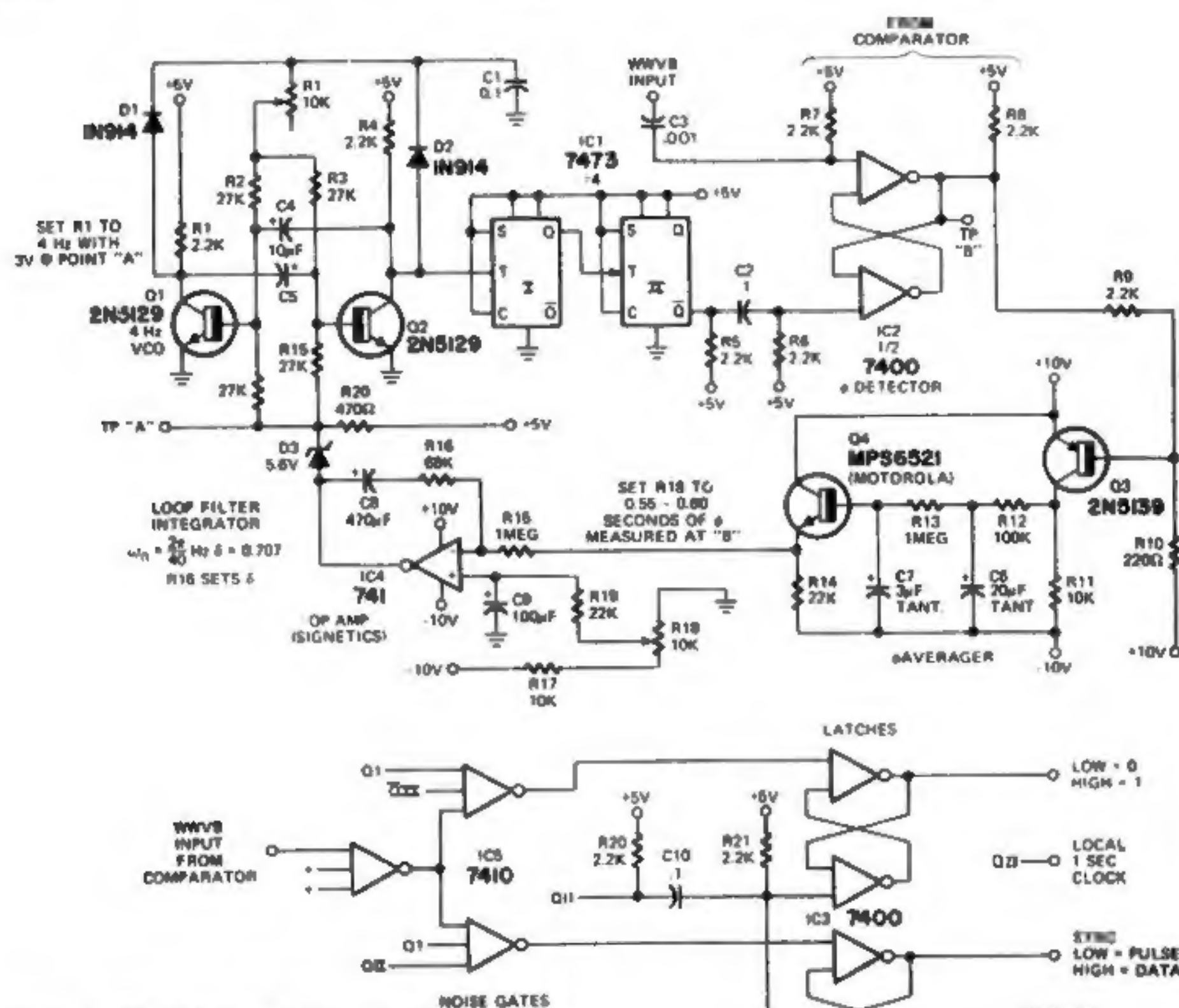


can SCR light dimmers, power tool controls, and worst of all, psychedelic lighting controls. In most locations you can work inside the building or in an attic crawl space, but get away from and above any and all metal. Some rotation of the antenna might eliminate directional interference. Be sure to try several locations if you seem to have local interference or reception problems.

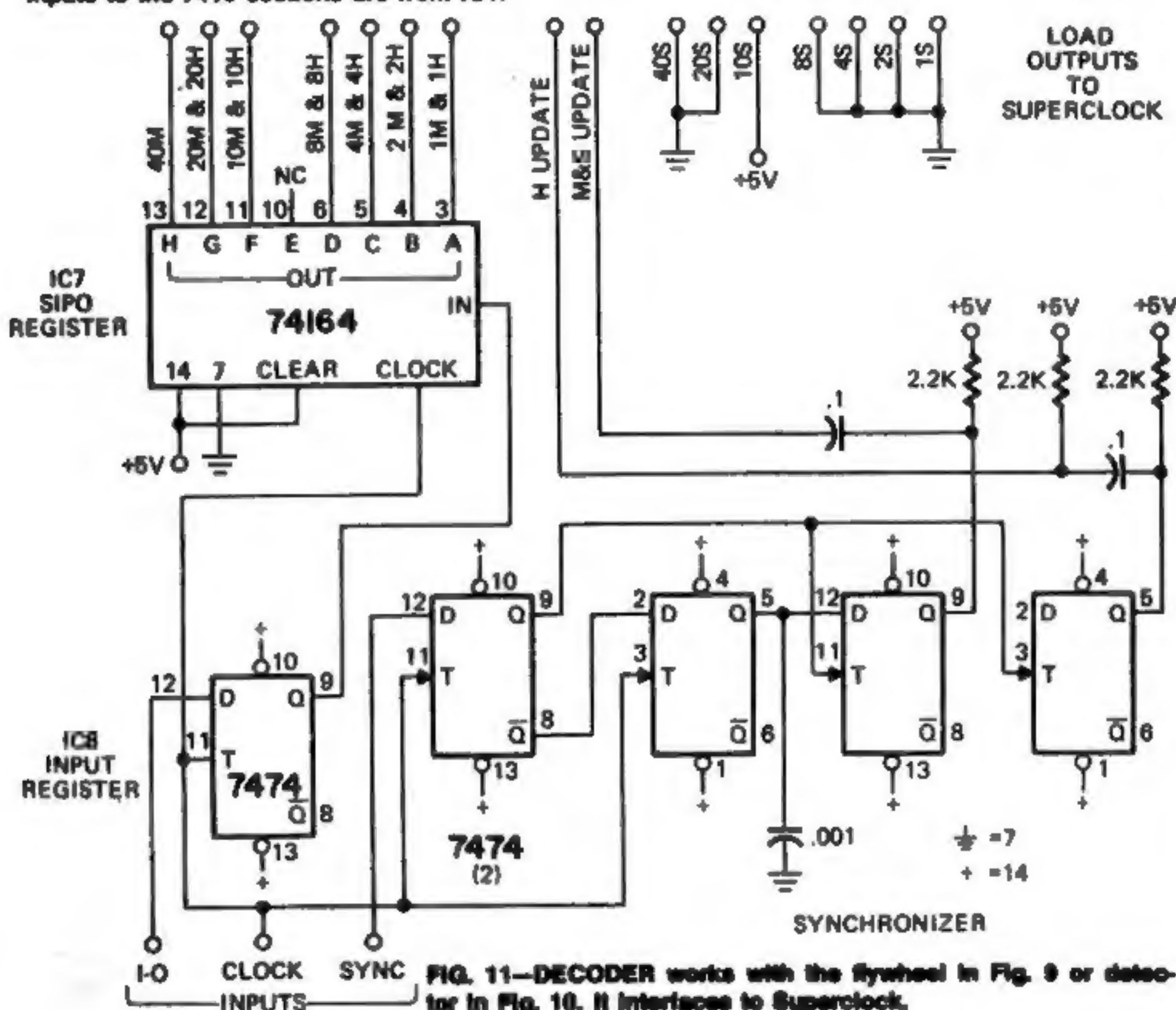
R-E

# PC BOARDS AND MORE SUPERCLOCK INFORMATION

Replicas of the PC boards for the Pre-amp (Fig. 4) and the Flywheel (Fig. 9) are available free from  
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 219 WEST RHAPSODY  
 SAN ANTONIO, TEXAS 78216  
 Complete Superclock Kits, PC boards, Time Zone chips and Time Zone conversion kits also remain available.



**FIG. 9—OPTIONAL PHASE LOCK**  
 "FLYWHEEL" output loop to minimize noise errors. The "Q" inputs to the 7410 sections are from IC1.



**FIG. 11—DECODER** works with the flywheel in Fig. 9 or detector in Fig. 10. It interfaces to Superclock.

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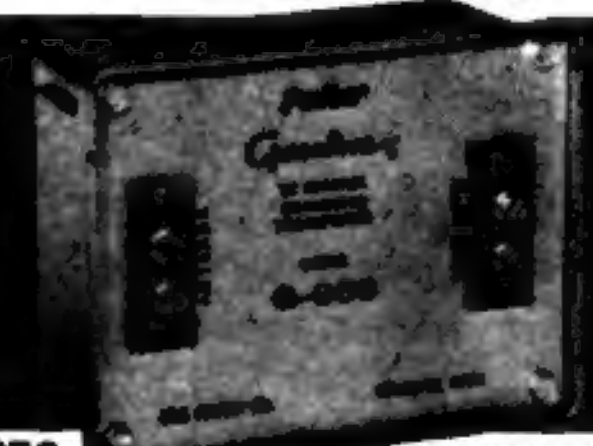
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